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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/809,749	03/25/2004	Brian Robert Prasky	POU920030065US1	7321

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EXAMINER	
FENNEMA, ROBERT E	
ART UNIT	PAPER NUMBER
2183	

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12/24/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/809,749	PRASKY ET AL.	
	Examiner	Art Unit	
	ROBERT E. FENNEMA	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 October 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-8 and 10 have been considered. Claims 11-18, 20-28, and 30 cancelled as per Applicant's request. Claim 1 amended as per Applicant's request.

2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 10/24/2008 has been entered.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 1- 8 and 10 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Applicant has claimed that a branch address is placed into a branch history table buffer, however, Examiner can find no recitation of this in the specification. On a careful review of the specification, the Applicant's usage of

the terms “Branch History Table” (BHT) (which is what Examiner assume the Branch History Table Buffer to be, as Applicant has no support for a Branch History Table Buffer either) and Branch Target Buffer (BTB) appear to be consistent with the common usage of the terms, where a prediction of taken or not taken is in the BHT, and the addresses are in the BTB. Applicant is required to cancel the unsupported matter from the claims, or to clearly indicate where in the specification support is for this amendment.

5. Claims 1-8 and 10 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Applicant has claimed that a Branch History Table Buffer holds an address of a branch, however, the Applicant’s specification clearly states that the BHT holds predictions of taken or not taken, and that the Branch Target Buffer is responsible for holding branch addresses. One of ordinary skill in the art would not be capable of making or using a BHT which can hold an address without undo experimentation, as neither the common usage, nor definition in the specification of the BHT permits allowing it to hold an address. Examiner is interpreting the claims as the specification lays out for the purposes of examination.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-8 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Check et al. (USPN 6,125,444, herein Check), in view of Patterson et al. (herein Patterson).

8. As per Claim 1, Check teaches: A method operating a computer having a pipelined processor (Figure 1), comprising setting a bit within an instruction text field of a branch (Column 2, Lines 33-40 and Column 4, Lines 24-27), but fails to teach:

said bit preventing the branch address from being placed into a branch history table buffer and a branch target buffer to thereby prevent the branch from being written into the branch history table buffer and branch target buffer and preventing the branch from being predicted and to make the branch only detectable as the time frame of decode.

While Check teaches using an instruction field of an instruction to disable a branch history table, he does not teach that doing so would prevent the branch from being placed in a branch target buffer, because Check is silent towards a branch target buffer even existing in the system. However, Patterson teaches that in order to further increase the performance of branches, a “branch target buffer” is often used, so that the

target address can be calculated in the fetch stage, instead of the decode stage (Pages 271-275). As the branch target buffer relies on having a prediction in order to determine the correct address, as seen by Figure 4.23 on Page 275, if no prediction was able to be generated, because of a BHT being disabled, then it would have been obvious to one of ordinary skill in the art to also not use the BTB, as it would not have the data it needs to be made use of, therefore, attempting to use a BTB in this situation would not only not make sense, but would be almost guaranteed to generate erroneous output. In addition, as can be seen by Column 2, Lines 28-31, sensitive system operations require cache control, so for the same reason Check disables the BHT, the BTB would need to not be written to as well. Given the advantage of a BTB as disclosed by Patterson, and the need to implement it in the system as disclosed by Check, one of ordinary skill in the art at the time the invention was made would have been motivated to include a BTB, and also to disable its use when the BHT was disabled, as the entire branch prediction mechanism must be disabled.

9. As per Claim 2, Check teaches: The method as defined in claim 1 comprising predicting the direction and target of a branch prior to decode (Figure 1).

10. As per Claim 3, Check teaches: A method as defined in claim 2 comprising predicting the direction and target of a branch prior to decode through a branch prediction array (Figure 1, also see Column 4, Lines 32-49).

11. As per Claim 4, Check teaches: A method as defined in claim 1 comprising tracking the branch from the beginning of the pipe, decode, until the time frame that the given instruction is to be written into a branch prediction array (It is inherent that instructions in a pipeline are kept track of, they must exist until they are removed).

12. As per Claim 5, Check teaches: A method as defined in claim 1 comprising denoting the instruction text field as a non-writable branch into the BTB (Column 2, Lines 36-40).

13. As per Claim 6, Check teaches: The method as defined in claim 5 comprising denoting the instruction text field in the system area as a non-writable branch into the BTB in system whereby the branch is blocked from being written to the BTB (Column 2, Lines 28-31).

14. As per Claim 7, Check teaches: The method as defined in claim 6 comprising predicting the branch via aliasing (Column 4, Lines 12-15).

15. As per Claim 8, Patterson teaches: The method as defined in claim 1 wherein machine state altering code lies within an address range spanned by branch tag bits of the branch target buffer (All instructions can alter machine state, so if any instruction is in the BTB, machine state altering code lies within an address range spanning by tag

bits in the BTB).

16. As per Claim 10, Check teaches: The method as defined in claim 8 comprising denoting state altering code in the system area by a state bit within the BTB/BHT such that aliasing of branches is prevented within the system area (Column 2, Lines 28-40).

Response to Arguments

17. On pages 11-12 of the remarks, Applicant has state that the Examiner does not understand the facts of the case, and then cites information from the Specification to argue why the cited references do not teach the claimed invention. However, Examiner notes that the specification is not what was rejected, and that the Applicant must argue what is in the claims, and to argue that the Examiner failed to note that the preferred embodiment does not disable other branch prediction mechanisms is completely immaterial, as there is no such recitation in the claims.

18. Applicant has also argued on Page 11 of the remarks that the Examiner has created a “straw man" argument in his combination of references, seemingly on the basis that because one reference was older than the other, that somehow there is no possible way that they could be combined, despite the teachings of Patterson being a textbook, teaching the most basic of concepts that all of skill in the art would readily recognize. Examiner sees absolutely no straw man argument, instead, Applicant appears to be arguing that the references cannot be combined due to one being older

than the other, which has absolutely no basis, and Examiner is not persuaded by these arguments.

19. Throughout the remaining arguments, it appears that the Applicant has not attempted to argue the Examiners mapping of the references to the claims, nor is there any argument as to why the Examiners combination of the references is incorrect, instead, there only appears to be an explanation of what the application does, and what the reference does, Applicant only appears to argue that the Examiner is incorrect, and Examiner is not persuaded by these arguments. The Examiner has laid out, very explicitly, and very clearly, why disabling one part of branch prediction, and not the other part, would result in catastrophic failure for the computer system, and would only serve to undermine the very purpose of disabling any kind of branch prediction in the first place. Applicant has not addressed what the Examiner has said, and the arguments that the Examiner is incorrect, without any specific evidence or arguments to the specific mappings that the Examiner has laid out, is not persuasive. Applicant's arguments also appear to be heavily based on limitations not found in the claims, and thus are not applicable to the Examiners rejection, and have no bearing on this case.

20. To further prosecution of the case, Examiner recommends either adding the limitations to the claims that the Applicant appears to have been arguing, or to make arguments and comments specifically on the Examiners rejection, in detail, as opposed to simply reciting the text of the specification of the application and of the reference,

which Examiner will not find persuasive, as there is no evidence or clear pointing out of any errors in the rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ROBERT E. FENNEMA whose telephone number is (571)272-2748. The examiner can normally be reached on Monday-Friday, 8:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Richard Ellis/
Primary Examiner, Art Unit 2183

RF